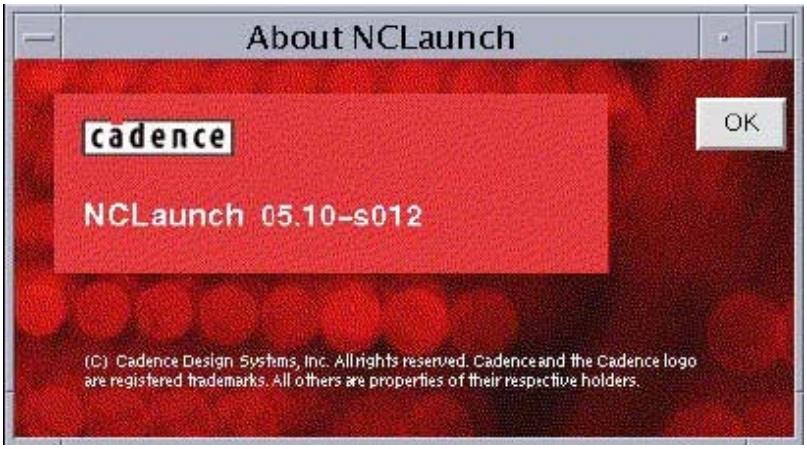
ELECTRICAL AND COMPUTER ENGINNERING DEPARTMENT,
UNIVERSITY OF CYPRUS

ECE 407/657 Computer Aided Design for VLSI

CADENCE NCLaunch Tutorial



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NCLaunch is a graphical user interface that allows for the management of large design projects and the configuration and launching of the Cadence simulation tools. This NCLaunch tutorial is intended for students to help them simulate Verilog, VHDL, or mixed-language designs using the NCLaunch tool. This tutorial explains the basic functionality of the tool and gives an example of simulating a VHDL module with NCLaunch. After finishing this tutorial, you will have a basic working knowledge of the main features of the simulator.

1. Remote Accessing

In order to start using NCLaunch you have to login to a specific machine running the application and having the appropriate configuration to do so. For this course this machine is ***Suadela***. The network identification for Suadela is:

Hostname: suadela.polytech.ucy.ac.cy **IP address:** 194.42.10.240

You will need this information in order to remotely login to this machine. The remote login configuration in the lab has been done, but you will need to configure remote login yourself, if you want to work from your home computer. To do so, you need a remote connection software such as X-Win for MS Windows, or any Linux/UNIX X-Windows environment, either as an emulator (cygwin) or a standalone operating system. Your username and password, for accessing Suadela, will be provided to you in the first laboratory by the laboratory coordinator. Moreover, you will need a VPN connection to access Suadela, (or any other University hosted machine) when connecting via any Internet Provided. You can download the Cisco VPN Client software provided by the University's Computer Center from: http://www.ucy.ac.cy/security/network.htm. The username and password for the VPN authentication is the same as it is for your email account. Note that the VPN Client software has to be executed before attempting to connect to Suadela, in order for the secure connection to be established.

2. Before Starting

When logging in to your account for the first time you will have to take some "first time" actions in order to eliminate potential problems when running the tool and make the tool easier to use.

After giving your Sudela username and password in the interactive session, you will be entered in Solaris Operating System, CDE (Common Desktop Environment). CDE is the standard X-Windows environment for UNIX systems. You are encouraged to change your password using the ***passwd*** command. Open a new terminal by following the path <mouse right click> → *Tools* → *Terminal*. The terminal runs the standard **sh** shell which is not as use-friendly as you may expect it to be. If you are not familiar with **sh** shell you may need to switch to a more easy-to-use shell. You can use csh, bash, and tcsh. For the later a very good configuration file (.tcshrc) can be found under $CDSDIR/ECE407 directory and it is recommended to copy that file in your home directory the first time you login Suadela. The command ***tcsh*** switches to the tcsh shell.

The first time you enter Suadela you have to make some configuration for the NCLaunch software. First make an new directory named **ece407.** Copy files **cds.lib** and **hdl.var** from directory $CDSDIR/ECE407 to your ece407 directory. These files are necessary for the NCLaunch tool to run. Next, type **nclaunch &** and the tool will be opened in a new window. You are now ready to start programming in VHDL, describing and simulating your designs. Before that you may need to make a small improvement to the programming procedure by changing the text editor used by NCLaunch. To do so go to menu *Edit* → *Preferences* and change the Editor Command to /usr/local/bin/gvim –c "syntax on". You will notice the difference as soon as you try to edit your first vhdl file.

3. Getting Started

In this tutorial you will go through a complete process of compiling and simulating a VHDL described design. When the NCLaunch tool opens in a new window you will notice that it is spit into 3 main windows (see Fig. 1). In your left-hand side you can see your working directory, in other words the directory from which you have run nclaunch. You can see all your files here and browse among directories. On your right-hand side you can see a list of the available libraries as well as the libraries you have created. The bottom window is a command-line interface that you will not be directly using, since all the command will be given by the nclaunch interface. Note that here you can see all the errors and warnings occurred when the tool compiles your designs.

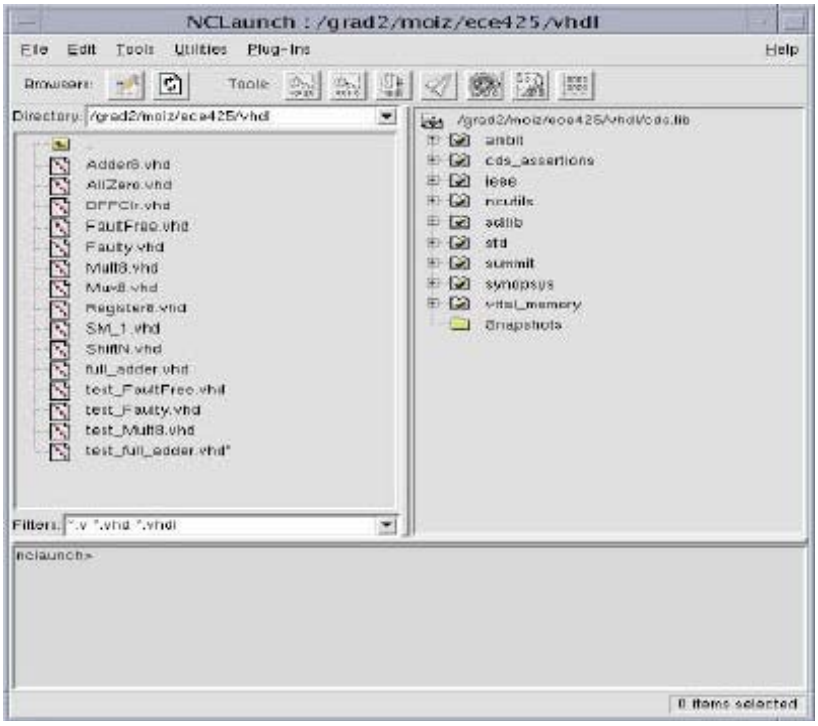


Figure 1. The NCLaunch Interface.

4. Setting Up the Working Directory/Library

Every new project you are starting should have its own working directory. That is a directory that holds all the files produced after compiling your design or when you are trying to simulate your design. To create a new working directory, go to menu *File* → *Set Design Directory*. In the pop-up window click on *New* and enter the name desired in the field *Library Name*. You can even pick an existing name when dealing with a number of different projects. For this tutorial give the name *work* to your library (if doesn't exist already, create it!). A new directory named *work* has been created in your ece407 directory and in the library list you can see the library you have just created tagged with a safety helmet icon (see Fig. 2).

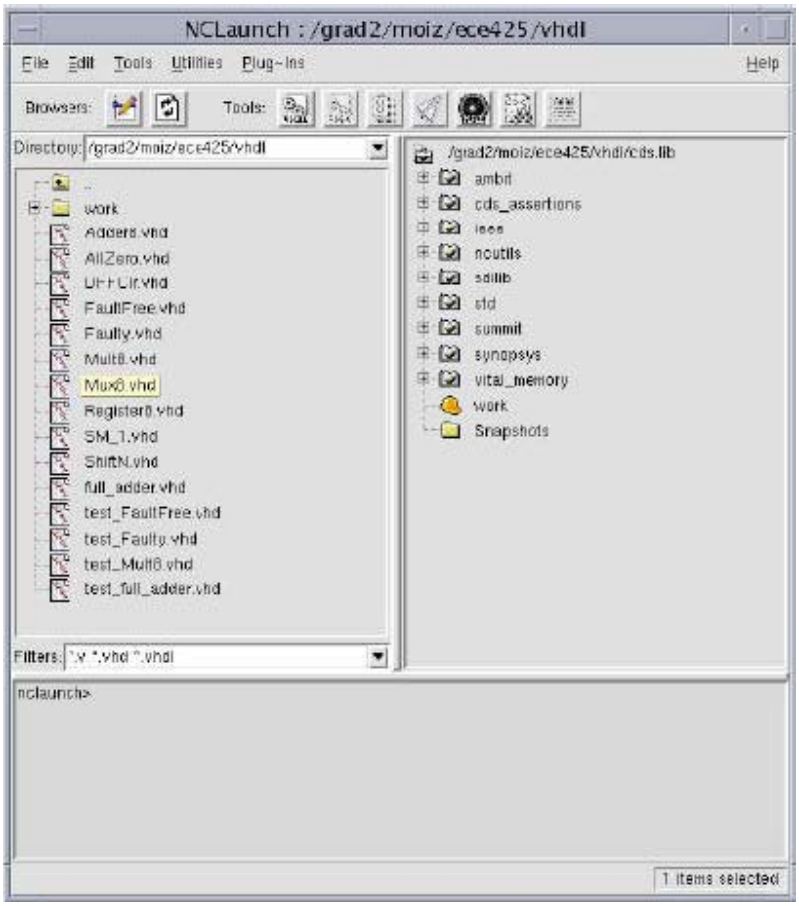


Figure 2. Work Library has been created.

5. Compiling and Linking your Design

You are now ready to compile you first VHDL design in the NCLaunch tool. First copy to your working directory the two files **AOI321.vhd** and **test_AOI321.vhd** from directory $CDSDIR/ECE407/. Observe that the files now appear on the left sub-window of NCLaunch. When you select a file you can perform a number of actions for that file.

For instance if you push the first button from the toolbar the file is edited in a new window editor. Have a look at the two files to understand the functionality of the design and the stimuli provided by the testbench. If you select *Tools → VHDL Compiler* then the compiler window will pop-up. Accept the parameters given in the various fields and your design will be compiled. Do that for the file AOI321.vhd. Alternatively, you can compile a design by double-clicking the file in your working directory. Do so for the test_AOI321.vhd file. Check the bottom sub-window to make sure you have no errors or warnings for your design. The later file is a *testbench* for the former file. A testbench is a file providing simulation stimuli for a design and in most cases its code is not synthesizable. After compilation the testbench should be "linked" to the design that is meant to test. In other words the test bench should be associated with the corresponding designs. This can be done by using the **Elaborator** command. In order to use this tool you have to locate the entities and their descriptions produced by the compilation. Go to the right sub-window of NCLaunch and expand the *work* library (Fig.3). This gives you the two entities you have compiled i.e. AOI321 and test_AOI321. If you expand them both you will see two objects: the entity declaration and the entity description. If either of the objects are not there this indicates an error in the compilation process. Select the test bench description (here *test*) and go to *Tools → Elaborator.* Accept the Elaborator's options and the linking process will begin. The result of the Elaboration process can be seen under the **Snapshots** folder in the library list.

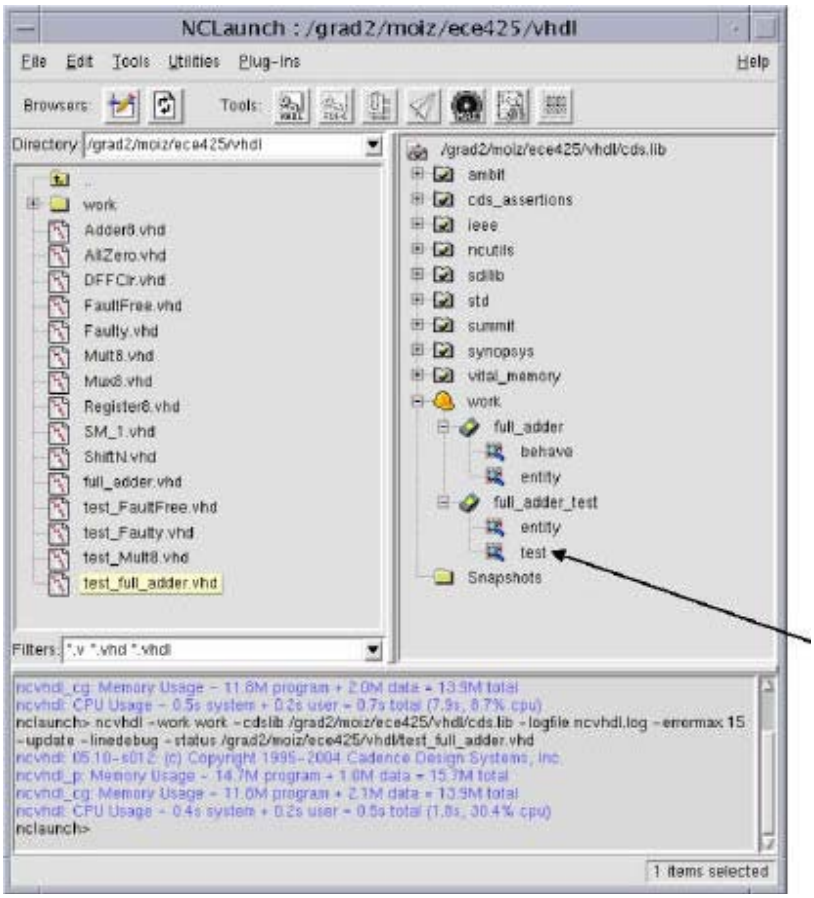
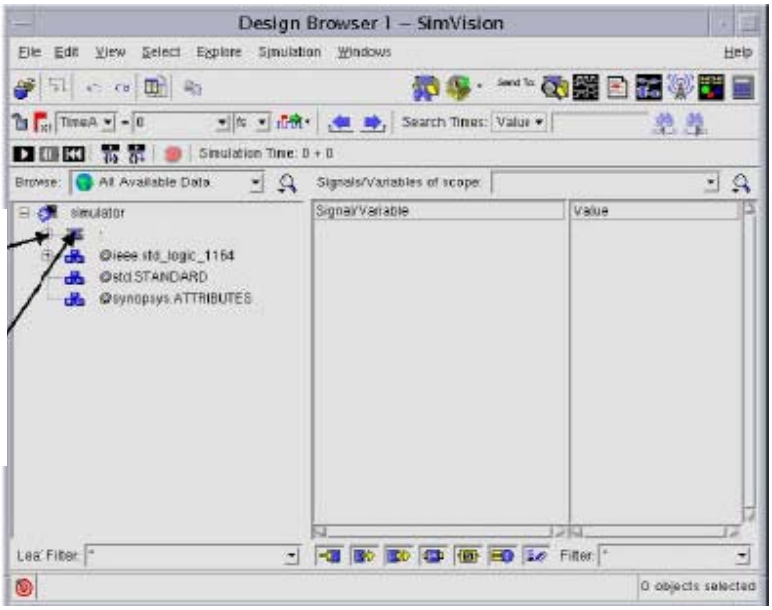


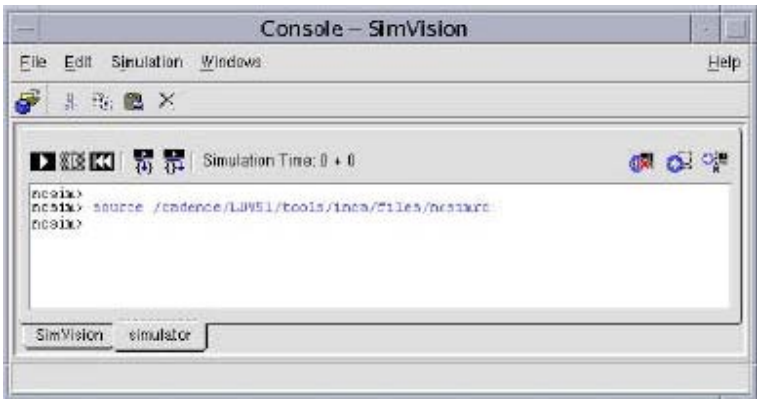
Figure 3. Selecting the testbench to Elaborate.

6. Simulation

If you carry out the Elaboration process successfully you can see a new object under the **Snapshots** folder. In this folder you can find all your compiled and linked designs. Any design under the Snapshot folder can be seen as a netlist of your design together with some logic values to be used as input stimuli for your design. Select the entity **work.test_AOI321:test** and then go to menu *Tools* → *Simulator*. Accept all options in the simulator pop-up window and the SimVision simulator will start. The later action may take some time. The resulting screen has two more windows: the **Design Browser** (Fig 4a) and the **Console** (Fig. 4b)**.** In the Design Browser select the desired component and open menu *Window* → *New* → *Waveform.* This pops up a new empty waveform window (Fig 5).



(a)



(b)

Figure 4. The Simulator Windows

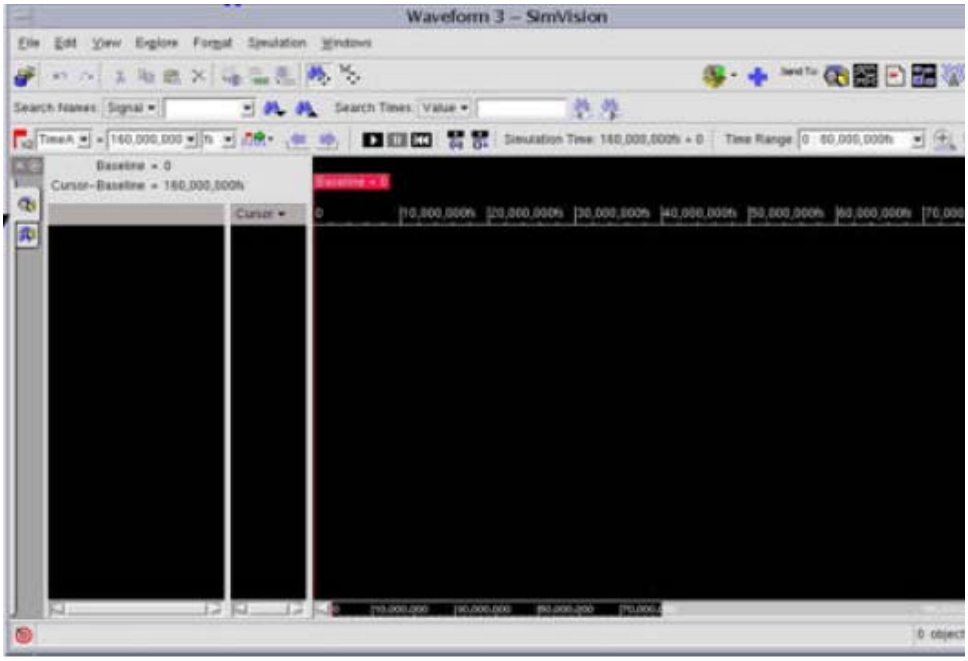


Figure 5. An empty waveform.

Now click on the first tab on the left side of the window to get the design browser. Select the primary inputs and the primary outputs you want to include in your simulation (Fig. 6). The selected ports will appear in the waveform area. You are now ready to start the simulation. Before doing so we have to set some breakpoints or else the simulation will be executed until an interrupted action is taken. To set a breakpoint go to *Simulation* → *Set Breakpoint* → *Time.* In the pop-up window set the breakpoint duration to 150ns since as you may remember the input stimuli is for 15 values, 10ns per value. Accept the value given.

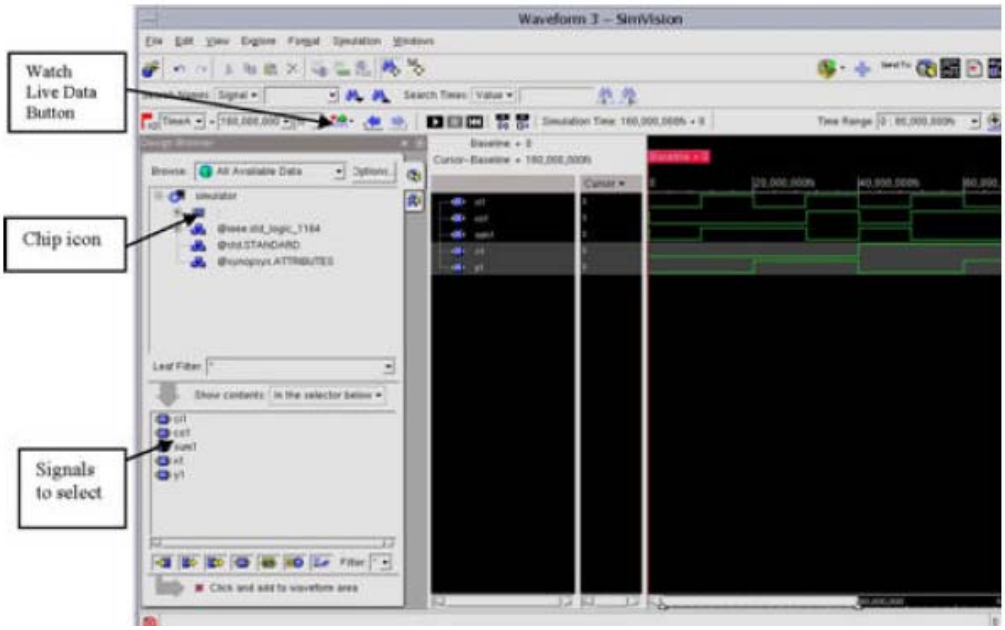


Figure 6. Execute simulation

Now run your simulation by clicking *Simulation* → *Run* or by clicking the **Run** button. The simulation will be executed in 150 ns steps. If you cannot see the simulation waveforms click the **Watch Live Data** button shown in Fig. 6. Adjust the simulation properly by zooming in and out to see the whole simulation period or the simulation time interval desired. In this window you can perform a number of actions including setting cursors, identifying components, locating ports in your design and so on. Try to explore the simulator capabilities by selecting the various options of this window. Give special attention to the *File* → *Export* option, which allows to save the results of the simulation in some specific formats.

7. The whole picture

When you are done exploring the tool, you can run the whole process of compiling, linking and simulating. Carry out the whole process for two more designs located in the $CDSDIR/ECE407 directory, i.e. half_adder.vhd and 2to1_MUX.vhd. Export the simulation results in a comma separated file, and show your results to the laboratory coordinator. When you are done close all the windows you have opened by clicking *File* → *Exit*.

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